

REMARKS

This paper responds to the Office Action mailed on December 29, 2006.

Claim 76 (second occurrence) is amended. Claims 13-16, 48-65, and 76-78 remain pending in this application.

Applicant maintains all arguments presented in the previous amendment and response. Applicant submits further arguments below. Applicant believes that the claims are patentable over the cited art. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of the claims.

Claim Objections

Mis-numbered claim 76 was objected to. Claim 76 (second occurrence) has been amended and renumbered as claim 78 per the Examiner's suggestion. Withdrawal of the rejection is respectfully requested.

Objection to the Official Notice

The Office Action cites a single document (Namekawa) to reject claims 13-16, 48-65, and 76-78 of the present application under 35 USC § 103(a) based on reasons that some of the specific features in these claims, although not disclosed in the single document, are obvious arrangement of parts. For example, the Office Action, pages 6 and 8, admits that Namekawa does not disclose the exact location of the switching units recited in claims 13 and 48. The Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to place the switching units of Namekawa between the second supply node and one of the internal node (to achieve the arrangement of switching units recited in claims 13 and 48), since it has been held that rearranging parts of an invention involves only routine skill in the art. Applicant submits that things recited in the claims, including the switching units in claims 13 and 48, are different from those taught by Namekawa. Therefore, Applicant respectfully traverses the rejection. Plus, Applicant assumes that the Examiner is taking Official Notice in rejecting these claims because the Office Action offers no documents to support the rejection of the specific features in these claims, such as the switching units in claims

13 and 48. Applicant respectfully traverses the taking of Official Notice and, pursuant to M.P.E.P. § 2144.03, Applicant requests documents or an affidavit to support the rejection. Moreover, Applicant cannot find in Namekawa a motivation to modify the teaching of Namekawa as proposed in the Office Action. In the absence of documents or an affidavit to support the rejection of claims 13-16, 48-65, and 76-78, Applicant requests reconsideration, withdrawal of the rejection, and allowance of these claims. Notwithstanding the objection to the taking of Official Notice, Applicant believes that claims 13-16, 48-65, and 76-78 are patentable over Namekawa for the reasons presented below.

§103 Rejection of the Claims

Claims 13-16, 48-65 and 76-78 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Namekawa (U.S. 6,115,301).

Applicant respectfully traverses for at least the reasons presented below.

Claim 13-16 and 76

Applicant believes that independent claim 13 is patentable over Namekawa because Applicant is unable to find in Namekawa everything recited in claim 13.

For example, Applicant is unable to find in Namekawa the things recited in claim 13 such as “plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes”. The Office Action points to column 7 lines 3-20 of Namekawa and asserts that Namekawa teaches a first supply node and a second supply node. This column 7 lines 3-20 of Namekawa describes a portion of a fuse circuit 81a (FIG. 2) of Namekawa. The Office Action does not specifically point out which nodes in fuse circuit 81a are being compared to the first and second supply nodes of claim 13. The Office Action relies on FIG. 1, element 10 to reject the “plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes” of claim 13. Element 10 in FIG. 1 of Namekawa shows a block diagram of a memory cell array. As discussed herein, since the Office Action does not specifically point out which nodes in fuse circuit 81a of FIG. 2 of Namekawa are being compared to the first and second supply nodes of claim 13, Applicant is unable to see how element 10 in FIG. 1 of Namekawa can include the thing recited in claim 13

such as “plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes”. Even if Applicant assumes that Vcc and ground in fuse circuit 81a of FIG. 2 of Namekawa are being compared to the first and second supply nodes of claim 13, Applicant cannot see how element 10 of FIG. 1 of Namekawa can include “plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes” because element 10 of Namekawa, as mentioned previously, is a memory cell array whereas fuse circuit 81a in FIG. 2 of Namekawa is another circuit (fuse circuit), which is different and separated from element 10 (memory cell array) of Namekawa.

In another example, Applicant is unable to find in Namekawa the things recited in claim 13 such as “each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes”. The Office Action compares the switches (e.g., SW10 or SW20) in switch circuit groups 50 and 60 of FIG. 1 of Namekawa to the switching units of claim 13. However, as shown in FIG. 1, each switch in switch circuit groups 50 and 60 of Namekawa is connected between a data line (e.g., one of RDL, and DL0 through DL15) and a data input/output line (one of IO0 through IO15) and *not* between the second supply node and one of the internal nodes. In contrast, claim 13 recites “each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes”.

Further, the Office Action admits that Namekawa does not disclose the exact location of the switching unit in FIG. 1 of Namekawa. To reject “each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes” of claim 13, the Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made to place the switching units of Namekawa between the second supply node and one of the internal node, since it has been held that rearranging parts of an invention involves only routine skill in the art. Applicant respectfully disagrees for at least three reasons. First, Applicant cannot find in Namekawa a teaching, fair suggestion, or motivation for rearranging the switching units of Namekawa as proposed by the Office Action. Second, Applicant cannot find in Namekawa how the switching units in switch circuit groups 50 and 60 of FIG. 1 of Namekawa can be rearranged (as proposed

by the Office Action) so that each of these switching units is connected in series with one of the memory segments in element 10 of FIG. 1 of Namekawa between the second supply node and one of the internal nodes. Third, since each of the switching units of FIG. 1 of Namekawa is connected between two lines (a redundant or data line and an input/output line) for the function of replacing a defective data line, rearranging each of the switching units of FIG. 1 Namekawa (as proposed by the Office Action) would destroy the function of each of the switching units of Namekawa. For example, with the proposed rearrangement, at one terminal of the switching unit, a supply node would take place of one of a redundant line, a data line, or an input/output line. Therefore, the rearranged switching unit would no longer be connected between two lines (between a redundant or data line and an input/output line). Thus, the rearranged switching unit of Namekawa (as proposed by the Office Action) would destroy the function of replacing a defective data line taught by Namekawa.

The reasons presented above demonstrate that claim 13 is patentable over Namekawa. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 13.

Dependent claims 14-16 and 76 depend from claim 13 and recite the things of claim 13. Thus, Applicant believes that claims 14-16 and 76 are patentable over Namekawa for at least the reasons presented above regarding claim 13, plus the additional things recited in claims 14-16 and 76.

Claim 48-57

Applicant believes that independent claim 48 is patentable over Namekawa because Applicant is unable to find in Namekawa everything recited in claim 48.

For example, for at least the reasons represented above regarding claim 13, Applicant is unable to find in Namekawa the things recited in claim 48 such as “each of the first switching units connecting in between the first supply node and one of the memory segments”.

In another example, for at least the reasons represented above regarding claim 13, Applicant is unable to find in Namekawa the things recited in claim 48 such as “each of the second switching units connecting between the second supply node and one of the memory segments”.

In another example, claim 48 recites “a first storage node and a second storage node”. The Office Action does not specifically points out in Namekawa which nodes are being compared to the first storage node and the second storage node of claim 48. Nevertheless, Applicant is unable to find in Namekawa “a first storage node and a second storage node”.

In another example, Applicant is unable to find in Namekawa the things recited in claim 48 such as “each of the memory cells including a latch connected to the first and second storage node and connected in between a first internal node and a second internal node”. The Office Action relies on column 1 lines 5-40 of Namekawa to reject “each of the memory cells including a latch connected to the first and second storage node and connected in between a first internal node and a second internal node” of claim 48. Column 1 lines 5-40 of Namekawa describes some background information about replacing a defective data line with a redundant data line. Applicant is unable to find in this column 1 lines 5-40 of Namekawa a teaching or fair suggestion of a plurality of memory segments, in which each of the memory segments includes a plurality of memory cells with each of the memory cells having a first storage node and a second storage node and “a latch connected to the first and second storage node and connected in between a first internal node and a second internal node”, as claimed in claim 48.

In another example, Applicant is unable to find in Namekawa the things recited in claim 48 such as “each of the memory cells including a first access element for accessing the first storage node”. The Office Action relies on column 6 lines 25-50 of Namekawa to reject “each of the memory cells including a first access element for accessing the first storage node”. Column 6 lines 25-50 of Namekawa describes operation of decode circuits 50 of FIG. 1 of Namekawa. Applicant is unable to find in this column 6 lines 25-50 of Namekawa a teaching or fair suggestion of a plurality of memory segments, in which each of the memory segments includes a plurality of memory cells with each of the memory cells having a first storage node and a second storage node and “a first access element for accessing the first storage node”, as claimed in claim 48.

In another example, Applicant is unable to find in Namekawa the things recited in claim 48 such as “each of the memory cells including a second access element for accessing the second storage node”. The Office Action relies on column 6 lines 25-50 of Namekawa to reject “each of the memory cells including a second access element for accessing the second storage node”. As

mentioned above, column 6 lines 25-50 of Namekawa describes operation of decode circuits 70 of FIG. 1 of Namekawa. Applicant is unable to find in this column 6 lines 25-50 of Namekawa a teaching or fair suggestion of a plurality of memory segments, in which each of the memory segments includes a plurality of memory cells with each of the memory cells having a first storage node and a second storage node and “a second access element for accessing the second storage node”, as claimed in claim 48.

The reasons presented above demonstrate that claim 48 is patentable over Namekawa. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 48.

Dependent claims 49-57 depend from claim 48 and recite the things of claim 48. Thus, Applicant believes that claims 49-57 are patentable over Namekawa for at least the reasons presented above regarding claim 48, plus the additional things recited in claims 49-57.

For example, claim 50 recites that at least one of the memory segments has “a circuit short between the first and second internal nodes”. The Office Action relies on column 4 lines 30-50 of Namekawa to reject claim 50. This column 4 lines 30-50 of Namekawa lists components of a device including, among other things, a memory cell array and a defective memory address for storing an address of a defective data line. Applicant is unable to find in column 4 lines 30-50 of Namekawa a teaching or fair suggestion **that** at least one of the memory segments of the memory cell array of Namekawa has “a circuit short between the first and second internal nodes”.

In another example, claim 53 recites that “each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments”. The Office Action relies on column 5 lines 37-50 of Namekawa to reject claim 53. This column 5 lines 37-50 of Namekawa describes a memory cell of memory cell array 10. Applicant is unable to find in column 5 lines 37-50 of Namekawa a teaching or fair suggestion of switching units in which “each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments”.

In another example, claim 55 recites that the latch includes “first inverter having an input node connected to the first storage node and an output node connected to the second storage

node” and “a second inverter having an input node connected to the second storage node and an output node connected to the first storage”. The Office Action relies on column 8 lines 25-40 of Namekawa to reject claim 55. This column 8 lines 25-40 of Namekawa describes some components of a decode circuit (e.g., D0 of FIG. 1 or FIG. 4). Applicant is unable to find in column 8 lines 25-40 of Namekawa a teaching or fair suggestion of a latch of a memory cell in which that latch includes a “first inverter having an input node connected to the first storage node and an output node connected to the second storage node” and “a second inverter having an input node connected to the second storage node and an output node connected to the first storage”

Claim 58-62 and 77

In rejecting claims 58-62, the Office Action does not specifically offer reasons why each and every element of claim 58 is rejected. The Office Action only states that claims 58-62 are system claims of claims 13-16 and 48-57 and are rejected for reasons set forth in claims 13-16 and 48-57. Applicant respectfully traverses. Applicant believes that independent claim 58 is patentable over Namekawa because Applicant is unable to find in Namekawa everything recited in claim 58.

For example, Applicant is unable to find in Namekawa the things recited in claim 58 such as a memory array connected to the supply node via “a supply path for receiving the voltage source”. Namekawa teaches a memory array cell 10 (FIG. 1). Applicant is unable to find in Namekawa a teaching or fair suggestion that memory array cell 10 of Namekawa is connected to a supply node via a supply path for receiving the voltage source.

In another example, Applicant is unable to find in Namekawa the things recited in claim 58 such as “a supply control circuit connected in the supply path” for “isolating a memory segment of the memory array from the supply node if the memory segment is defective”. Namekawa teaches a memory array cell 10 (FIG. 1) and replacing a defective data line with a redundant data line. Applicant is unable to find in Namekawa a teaching or fair suggestion of a supply control circuit connected in the supply path or isolating a memory segment in memory array cell 10 of Namekawa from a supply node if the memory segment in array cell 10 is defective.

The reasons presented above demonstrate that claim 58 is patentable over Namekawa. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 58.

Dependent claims 59-62 and 77 depend from claim 58 and recite the things of claim 58. Thus, Applicant believes that claims 59-62 and 77 are patentable over Namekawa for at least the reasons presented above regarding claim 58, plus the additional things recited in claims 59-62 and 77.

Claim 63-65 and 68

In rejecting claims 63-65, the Office Action does not specifically offer reasons why each and every element of claim 63 is rejected. The Office Action only states that claims 63-65 are method claims of claims 13-16 and 48-57 and are rejected for reasons set forth in claims 13-16 and 48-57. Applicant respectfully traverses. Applicant believes that independent claim 63 is patentable over Namekawa because Applicant is unable to find in Namekawa everything recited in claim 63.

For example, Applicant is unable to find in Namekawa the things recited in claim 63 such as “isolating a memory segment of the memory device from a supply source if the memory segment is defective”. Namekawa teaches a memory array cell 10 (FIG. 1) and replacing a defective data line with a redundant data line. Applicant is unable to find in Namekawa a teaching or fair suggestion of isolating a memory segment in memory array cell 10 of Namekawa from a supply node if memory segment in array cell 10 is defective.

The reasons presented above demonstrate that claim 63 is patentable over Namekawa. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 63.

Dependent claims 64-65 and 78 depend from claim 63 and recite the things of claim 63. Thus, Applicant believes that claims 64-65 and 78 are patentable over Namekawa for at least the reasons presented above regarding claim 63, plus the additional things recited in claims 64-65 and 78.

For example, claim 65 recites that “isolating the memory segment includes electrically disconnecting the memory segment from the supply source”. Namekawa teaches in FIG. 1 a

memory cell array 10. Applicant is unable to find in Namekawa a teaching or fair suggestion of isolating a memory segment of the memory cell array 10 device from a supply source if the memory segment is defective, and isolating the memory segment of the memory cell array 10 includes electrically disconnecting the memory segment from a supply source.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

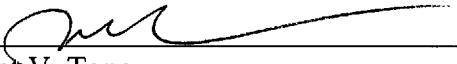
Respectfully submitted,

KENNETH W. MARR

By his Representatives,

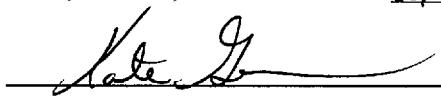
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 3/29/2007

By 
Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 29 day of March 2007.

Kenneth W. Marr
Name


Signature